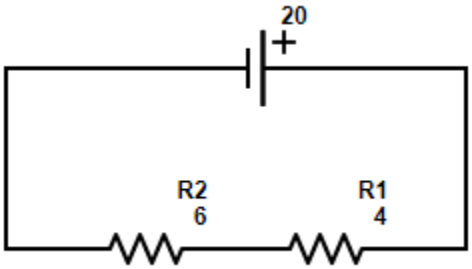
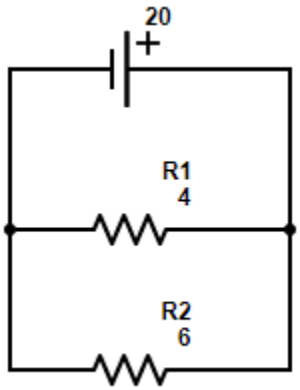
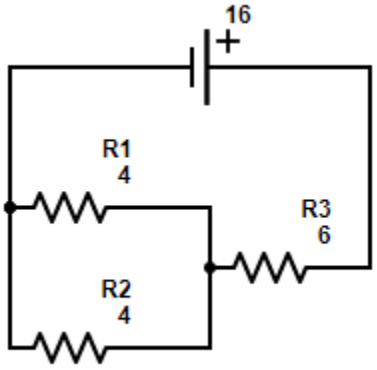
Circuit Reduction and Expansion



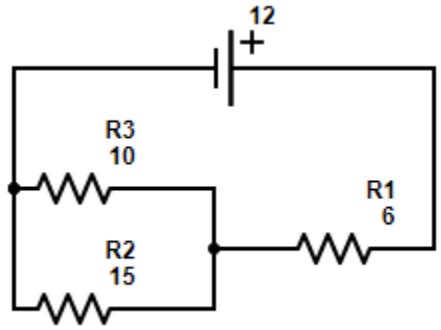
	V	I	R	P
Source	20			
R_1			4	
R_2			6	



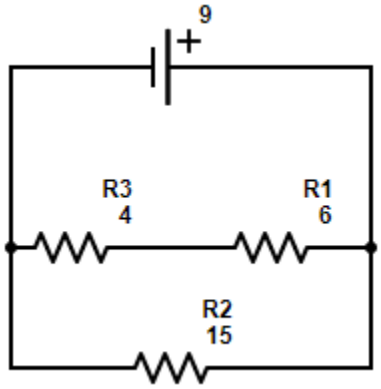
	V	I	R	P
Source	20			
R_1			4	
R_2			6	



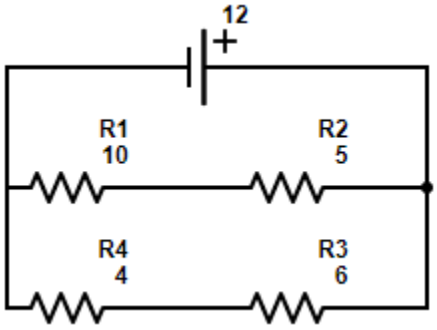
	V	I	R	P
Source	16			
R_1			4	
R_2			4	
R_3			6	



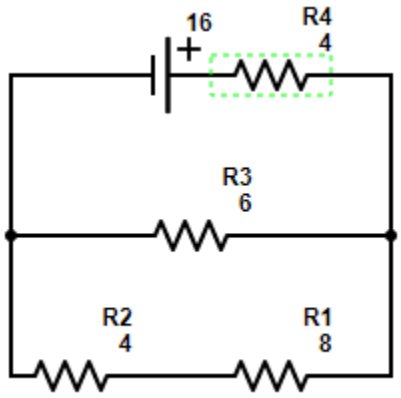
	V	I	R	P
Source	12			
R_1			6	
R_2			15	
R_3			10	



	V	I	R	P
Source	9			
R_1			6	
R_2			15	
R_3			4	



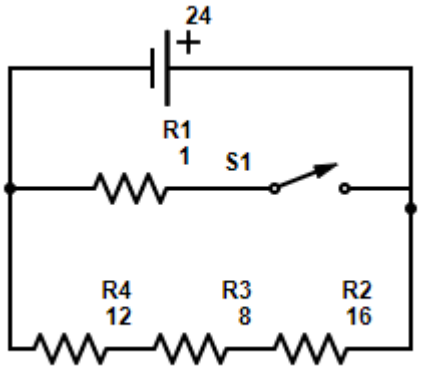
	V	I	R	P
Source	12			
R_1			10	
R_2			5	
R_3			6	
R_4			4	



	V	I	R	P
Source	16			
R_1			8	
R_2			4	
R_3			6	
R_4			4	

S1 is Open

	V	I	R	P
Source	24			
R_1			1	
R_2			16	
R_3			8	
R_4			12	

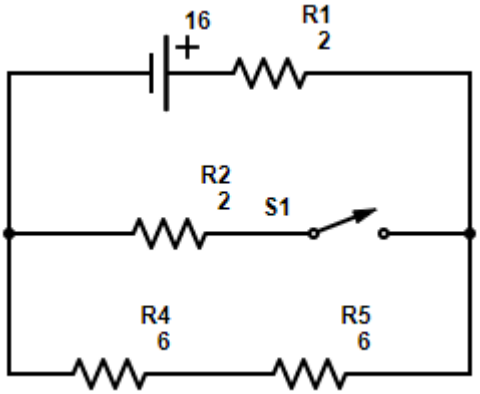


S1 is Closed

	V	I	R	P
Source	24			
R_1			1	
R_2			16	
R_3			8	
R_4			12	

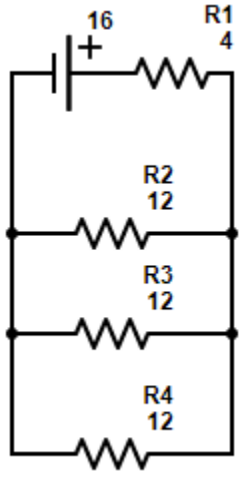
S1 is Open

	V	I	R	P
Source	16			
R_1			2	
R_2			2	
R_3			6	
R_4			6	



S1 is Closed

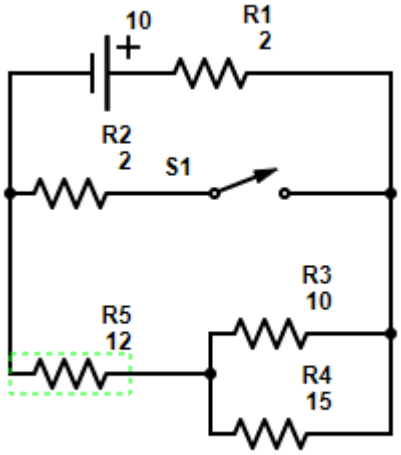
	V	I	R	P
Source	16			
R_1			2	
R_2			2	
R_3			6	
R_4			6	



	V	I	R	P
Source	16			
R_1			4	
R_2			12	
R_3			12	
R_4			12	

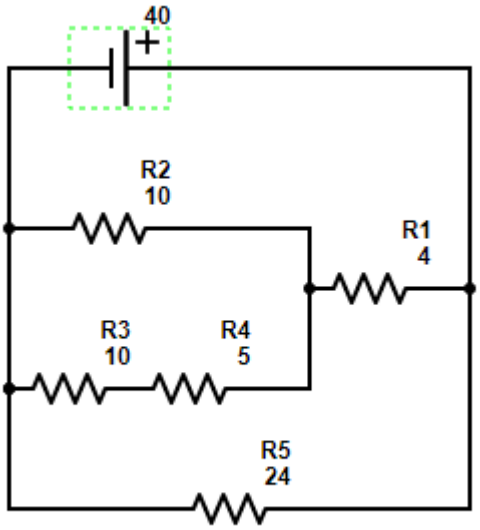
S1 is Open

	V	I	R	P
Source	10			
R_1			2	
R_2			2	
R_3			10	
R_4			15	
R_5			12	



S1 is Closed

	V	I	R	P
Source	10			
R_1			2	
R_2			2	
R_3			10	
R_4			15	
R_5			12	



	V	I	R	P
Source	40			
R_1			4	
R_2			10	
R_3			10	
R_4			5	
R_5			24	